MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

EEE4186 - VLSI SYSTEM DESIGN AND MODELING TECHNIQUE

(EE)

2 MARCH 2016
02.30p.m – 04.30p.m
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of 5 pages including cover page with 4 Questions only.

2. Attempt ALL FOUR questions. All questions carry equal marks and the distribution of the marks for each question is the same.

3. Please print all your answers in the answer Booklet provided.

4. A VHDL model means an entity-architecture pair, plus any extra codes that might be necessary for them to work properly (library, use, etc.)

5. When names (of entities, architectures, signals, etc.) are not specified, you may use any suitable and valid name.

Question 1

(a) There are specific structural elements which are responsible for forming the different parts of the hardware structure to model hardware by using VHDL coding. Describe and elaborate these structural elements such as ***entity***, ***architecture***, ***configuration*** and ***package***. [8 marks]

(b) The VHDL *structural* code of D flip-flop is shown in Figure Q1.
(i) Sketch the structural or logic diagram to show its construction.

[8 marks]

(ii) Write the VHDL *behavioral* code of D flip-flop with asynchronous active low *set_n* and *rst_n* inputs, which mean when *set_n* = '0', *Q* = '1', and when *rst_n*= '0', *Q* = '0'. (*entity* name: *d_ff*, *architecture* name: *Behavior*)

[9 marks]

```
entity d_ff is
    port (
    clk, rst_n, set_n, d: in  std_logic;
    q, q_n    : out std_logic);
end d_ff;

architecture struct of d_ff is
component nand
  port (    a, b, c : in  std_logic;
                y         : out std_logic);
end component;
signal y0, y1, y2, y3: std_logic;
signal y4 : std_logic;
signal y5 : std_logic;

begin  -- struct
  q     <= y4;
  q_n   <= y5;
  nand0 : nand port map (set_n,  y1,    y3,  y0 );
  nand1 : nand port map (clk,   rst_n,  y0,  y1 );
  nand2 : nand port map (clk,   y3,   y1,  y2 );
  nand3 : nand port map (d,  rst_n,  y2,  y3 );
  nand4 : nand port map (set_n,  y1,    y5,  y4 );
  nand5 : nand port map (rst_n,  y2,    y4,  y5 );
end struct;
```

Figure Q1

Continued ...

Question 2

(a) Write the complete *architecture* of VHDL code to realize the signal bus condition as shown in Figure Q2a using the following signal assignment operator or method.

(i) Concatenation operator. [3 marks]

(ii) Aggregates method. [3 marks]

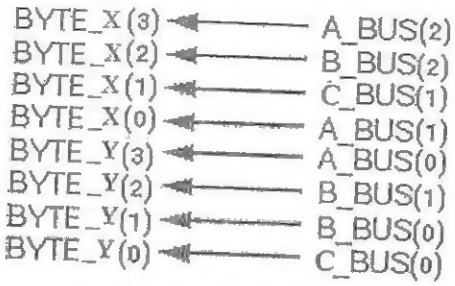

Figure Q2a

(b) Consider the circuit diagram shown in Figure Q2b below.

(i) Write down the *entity* declaration of this circuit. (*entity* name: *unknown*) [5 marks]

(ii) Write the complete VHDL *architecture* code to represent the functional of this circuit using *if-else* statement. All outputs will be zero if EN='0'. (*architecture* name: *arch_1*)

[7 marks]

(iii) Write the complete VHDL *architecture* code to represent the functional of this circuit using *case* statement. Default outputs will be zero if EN='0'. (*architecture* name: *arch_2*)

[7 marks]

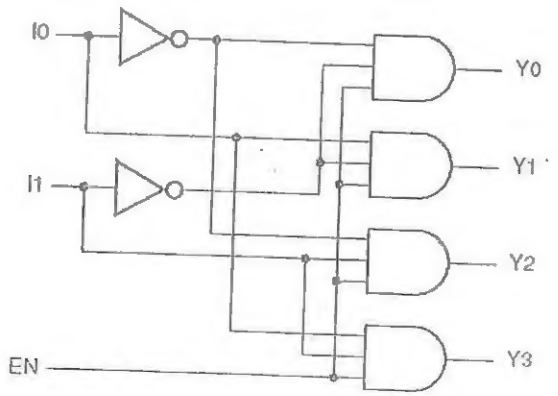

Figure Q2b

Continued ...

Question 3

(a) Sketch the circuit diagram for the synthesized VHDL code shown in Figure Q3 using 2-to-1 multiplexers and standard logic gates.

[9 marks]

```
entity cct1 is
port (A, B, x, y, z: in std_logic;
      dout: out std_logic);
end cct1;

architecture beh of cct1 is
begin
   dout <= A when x = '0' else
           B when y = '1' and z = '0' else '0';
end beh;
```

Figure Q3

(b) Compute the output signal, dout values of the circuit in part (a) corresponding to the input signals shown in Table Q3.

Table Q3

A	B	x	y	z
0	0	0	0	0
1	0	0	0	0
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1

[6 marks]

(c) Create a test bench in VHDL code to test the circuit in part (a), by referring to the work.cct1(beh). Test the circuit in part (a) using the input signals shown in Table Q3 and stop. The time step for the test bench is 100ns.

[10 marks]

Continued ...

Question 4

(a) Sketch the block diagram for the VHDL code shown in Figure Q4 using adder "+", subtractor "-" and registers.

[9 marks]

```
use work.my_package.all;
-- my_package contains "+" and "-" for bit_vectors

entity my_rtl is
port (clk: in bit;
      a, b, c: in bit_vector(3 downto 0);
      r: out bit_vector(3 downto 0));
end my_rtl;

architecture arch of my_rtl is
signal temp_a, temp_b, temp_c: bit_vector(3 downto 0);
begin
    process (clk)
    begin
        if clk'event and clk = '1' then
            temp_a <= a;
            temp_b <= b;
            temp_c <= c;
            r <= temp_a + temp_b - temp_c;
        end if;
    end process;
end arch;
```

Figure Q4

(b) Redesign the VHDL code in Figure Q4 to increase its maximum frequency using the pipelining technique. Given that the worst-case delay of the adder "+" operation is 0.5 ms and the delay of the subtractor "-" operation is 0.8 ms.

[12 marks]

(c) Compute the worst case delay and maximum frequency of the system in part (b).

[4 marks]

End of Paper